SEMICONDUCTOR DEVICE INCORPORATING A DEFECT CONTROLLED STRAINED CHANNEL STRUCTURE AND METHOD OF MAKING THE SAME

RELATED APPLICATION

[0001] This is related to United States Patent Application Number __/___,___ filed concurrently herewith, and entitled "Semiconductor Structure with Different Lattice Constant Materials and Method for Forming the Same" (Attorney Docket SC12626ZP) and is incorporated herein by reference and assigned to the current assignee hereof.

BACKGROUND

Field of the Invention

[0002] The present invention relates generally to semiconductor devices and method of making the same, and more particularly, to a semiconductor device incorporating a defect controlled strained channel structure and method of making the same.

Related Art

[0003] In the manufacture of semiconductor devices, various isolation structures for CMOS and methods of fabrication are known. One type of isolation structure includes inverse slope isolation. With respect to inverse slope isolation, it possesses a high probability of not terminating defects, for example, from the deposition of SiGe on Si, on a sidewall of the isolation. In addition, fabrication of a sloped sidewall isolation structure is difficult with current process tools and may not be controllable enough for manufacturing.

[0004] Accordingly, an improved semiconductor structure and method of making the same is desired.

SUMMARY

[0005] According to one embodiment, a semiconductor device includes a single crystal substrate and a dielectric layer overlying the substrate. The dielectric layer includes at least one opening having a first portion and an overlying second portion. The first portion has a depth and width, such that an aspect ratio of the depth to width is greater than one. The semiconductor device further includes a first material having a first portion and a second portion, the first portion of the first material filling the first portion of the at least one opening. Defects for relaxing strain at an interface between the first material and the substrate

material exist only within the first portion of the first material due to the aspect ratio being greater than one. The second portion of the first material is substantially defect free. Furthermore, the second portion of the first material and an overlying second material different than the first material fill the overlying second portion of the at least one opening. The second material has a thickness which is less than a critical thickness to maintain the second material in a strained state. The strained second material functions as a channel for charge carriers. Additional embodiments are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The embodiments of the present disclosure are illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

[0007] Figure 1A is a cross-sectional view of one stage in a process of making a semiconductor device incorporating a defect controlled strained channel structure according to an embodiment of the present disclosure;

[0008] Figure 1B is a top view of the structure of Figure 1A;

[0009] Figures 2-3 are cross-sectional views of various additional stages in a process of making a semiconductor device incorporating a defect controlled strained channel structure according to an embodiment of the present disclosure;

[0010] Figure 4 is a cross-sectional view of a semiconductor device including transistors incorporating a defect controlled strained channel structure according to an embodiment of the present disclosure;

[0011] Figure 5 is a cross-sectional view of a portion of a process of making a semiconductor device incorporating a defect controlled strained channel structure according to another embodiment; and

[0012] Figure 6 is a cross-sectional view of a semiconductor device including transistors incorporating a defect controlled strained channel structure according to another embodiment of the present disclosure.

[0013] Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve an understanding of the embodiments of the present disclosure.

DETAILED DESCRIPTION

[0014] Figures 1-3 are cross-sectional views of various stages in a process of making a semiconductor device incorporating a defect controlled strained channel structure according to an embodiment of the present disclosure. As shown in Figure 1A, semiconductor device 10 includes a substrate 12 and a dielectric layer 14 overlying the substrate. Substrate 12 includes any single crystal substrate, for example, a bulk silicon substrate, an SOI substrate, silicon on sapphire, or the like. Dielectric layer 14 includes any suitable dielectric layer, for example, a silicon dioxide, oxides, nitrides, or the like.

[0015] Locations of defect controlled strained channel structures, yet to be fabricated, are shown in Figure 1A and 1B as indicated by reference numerals 16, 18, and 20. An active region opening 22 is disposed over a substrate via 24, in location 20. Similarly, an active region opening 26 is disposed over both substrate vias 28 and 30, corresponding to locations 16 and 18, respectively. Figure 1B is a top view of the structure of Figure 1. For a given defect controlled strained channel structure location, the corresponding substrate via is characterized by a width dimension "w" and a depth dimension "d." In one embodiment, the aspect ratio of d/w is greater than 1.

[0016] Formation of the active region opening and the underlying substrate can be performed in any order, using any suitable conventional patterning and etching techniques. In one embodiment, an active region opening is formed prior to the underlying substrate via. As a result, undesirable rounding of corners of the underlying substrate via can be substantially reduced. For example, by forming the active region opening 22 first, followed by forming of the substrate via 24, corner 32 will include a substantially sharp well defined corner, that is, more than if the substrate via had been formed prior to the active opening. Formation of active region opening 26 and substrate vias 28, 30 can be similarly formed. The particular dimensions of an active region opening and an underlying substrate via are determined according to the particular requirements of a semiconductor device design, so long as the aspect ratio of d/w, of an individual substrate via of a given location of a defect controlled strained channel structure, is greater than 1.

[0017] In Figure 2, a single crystal semiconductor material 34 is epitaxially grown selectively with respect to the dielectric layer 14, using any suitable epitaxial growth technique. The single crystal semiconductor material 34 is selected to promote formation, or allow the achievement, of a desired strained layer in a defect controlled strained channel structure made according to an embodiment of the present disclosure. For example, the single crystal semiconductor material may include SiGe.

[0018] Epitaxial growth begins with deposition of the single crystal semiconductor material occurring on exposed surfaces of the underlying substrate 12 within a bottom portion of a respective substrate via, without growth on the sidewalls of the dielectric 14. During an initial growth period, defects begin forming within the epitaxial growth in response to the growth reaching or attaining a first critical thickness within a respective substrate via. Subsequent to the epitaxial growth exceeding the critical thickness, defects form in a region extending from the bottom of a respective substrate via and propagating at a material dependent angle until the defects reach and are terminated by a sidewall of the substrate via. For example, with respect to SiGe epitaxially grown over silicon, the propagation angle for defects is on the order of approximately 45 degrees. As shown in Figure 2, defects are included within defect filled regions of the substrate vias as indicated by reference numerals 25, 29 and 31, corresponding to substrate vias 24, 28 and 30, respectively.

[0019] Subsequent to the defects propagating and reaching the sidewalls of the substrate vias, the epitaxial growth thereafter continues defect free so as to fill the remainder of the substrate vias and corresponding overlying active region openings with defect free epitaxial growth. Accordingly, defect free regions are formed, otherwise referred to herein as relaxed regions. Furthermore, with respect to the epitaxial growth in the active region openings, and subsequent to being planarized, the defect free epitaxial growth enables the formation of relaxed active regions. As shown in Figure 2, epitaxial growth of material 34 is continued until a desired lateral overgrowth is achieved. The lateral overgrowth of material 34 in the locations 16 and 18 abut one another and form a seam 36. The lateral overgrowth of material 34 in the locations 18 and 20 are not required to abut one another, leaving a gap 38.

[0020] The structure of Figure 2 is then planarized at least down to a top surface of dielectric layer 14 using any suitable planarization technique. For example, the planarization technique may include CMP, etch back, or the like. In one embodiment, the structure of Figure 2 is planarized with CMP, such that a top portion of the epitaxially grown material in a corresponding active region opening location is slightly recessed with respect to the top surface of dielectric 14, forming corresponding active region epi as indicated by reference numeral 40 in Figure 3.

[0021] A strained layer 42 is then formed upon the active region epi 40. In one embodiment, formation of the strained layer 42 is accomplished by a process of a selective epitaxial deposition of a single crystal silicon material. For example, the single crystal layer 42 can include epitaxial silicon on a SiGe active region 40. Growth of the single crystal material in layer 42 is controlled to within a critical thickness, wherein the critical thickness corresponds to a not-to-exceed thickness that is sufficient to maintain layer 42 as a strained layer. In the example of a strained Si layer on a SiGe relaxed layer, the critical thickness is on the order of approximately 100 angstroms for a SiGe relaxed layer composed of 70% Si and 30% Ge. A surpassing of the critical thickness results in defect formation and relief of the corresponding strain.

[0022] Figure 4 is a cross-sectional view of a semiconductor device including transistors incorporating a defect controlled strained channel structure according to an embodiment of the present disclosure. Standard processing techniques can be used to form various transistor devices on the formation of the structure shown in Figure 3, according to the requirements of a particular semiconductor device design. For example, transistors 50, 52 and 54, can be formed as shown in Figure 4. According to one embodiment, each transistor 50 and 52 includes a gate dielectric 60, gate electrode 62, source/drain extension structures 64, sidewall spacers 66, source/drain regions (68,70). In addition, as shown in Figure 4, transistors 50 and 52 abut one another at seam 36, creating a common source/drain region between the transistors 50 and 52. The common source/drain region allows for an increased device packing density for semiconductor device 10. Since there is no junction crossing seam 36, any defects or crystal misalignment that may occur at this seam will not degrade device performance or increase device leakage. Transistor 54 can be similar to either of transistors 50 and 52, or different.

[0023] Figure 5 is a cross-sectional view of a portion of a process of making a semiconductor device incorporating a defect controlled strained channel structure according to another embodiment. In particular, Figure 5 is substantially similar to the structure shown in Figure 1A, with the following difference. Semiconductor device 10' includes a second dielectric layer 15 disposed on a top surface of first dielectric layer 14. In one embodiment, active region openings (22,26) are patterned in dielectric layer 15, followed by patterning of substrate vias (24,28,30) in dielectric layer 14, using any suitable patterning and etch techniques. A benefit of the embodiment of Figure 5 is that the second dielectric layer 15 facilitates an improved control of the depth of the active region openings. That is, the second dielectric layer 15 can be selectively etched with respect to the underlying dielectric layer 14, to form the desired active region openings. In addition, formation of the substrate vias subsequent to the active region openings facilitates sharp corner edges at the tops of the substrate vias, as previously discussed herein above. The structure of Figure 5 is then processed similarly as discussed with respect to Figures 2-4 above.

[0024] Figure 6 is a cross-sectional view of a semiconductor device including transistors incorporating a defect controlled strained channel structure according to another embodiment of the present disclosure. The structure of Figure 6 is similar to that shown in Figure 4, with the following differences. Subsequent to the transistor formation, various regions are silicided, for example, source/drain regions and gate electrodes, as indicated generally by reference numeral 80. Subsequent to the formation of the silicide regions, another dielectric layer 82 is formed overlying the semiconductor device structure 10' and planarized, using conventional techniques. Contact holes or openings 84 are formed, by conventional patterning and etching techniques, overlying desired contact areas. In one embodiment, dielectric layer 82 comprises a material different from dielectric layer 15. For example, layers 82 and 14 can include silicon dioxide, whereas dielectric layer 15 can include silicon nitride. Accordingly, with the use of a selective etch, dielectric layer 15 prevents the formation of undesirable etching of the dielectric material in region 86 next to an active region, in the event of any misalignment of a contact hole, during formation of respective contact holes 84.

[0025] Accordingly, a semiconductor device of the present disclosures includes a single crystal substrate formed of a substrate material. A dielectric layer overlies the single crystal substrate. The dielectric layer includes at least one opening that has a first portion and an overlying second portion. The first portion has a predetermined depth and a predetermined

width, such that an aspect ratio of the predetermined depth to the predetermined width is greater than one. The semiconductor device further includes a first material having a first portion and a second portion, the first portion of the first material filling the first portion of the at least one opening. Defects for relaxing strain at an interface between the first material and the substrate material exist only within the first portion of the first material due to the aspect ratio being greater than one. Accordingly, the second portion of the first material is substantially defect free.

[0026] The semiconductor device further includes the second portion of the first material and an overlying second material different than the first material filling the overlying second portion of the at least one opening. The second material has a thickness which is less than a critical thickness to maintain the second material in a strained state. Lastly, the strained second material functions as a channel for charge carriers.

[0027] In one embodiment of the semiconductor device, part of the second portion of the first material is laterally extended beyond the at least one opening to form a T-shape structure. T-shape structures are formed of a respective substrate via and corresponding overlying active areas. In one embodiment, the substrate vias connect the corresponding active areas to the underlying substrate and are well suited for terminating defects arising from the epitaxial deposition, for example, of SiGe on Si.

[0028] Accordingly, large area active structures can be fabricated while having defects terminate below the active device areas. The T-shape structure allows low leakage SOI-like source/drain structures to be fabricated with channels tied to the substrate, alleviating floating body issues while still retaining the low source/drain leakage to the well associated with SOI devices. In addition, a control electrode can be formed on the T-shape structure overlying a predetermined portion of the second material. A first current electrode is formed in the second material and offset from a first side of the control electrode. Lastly, a second current electrode is formed in the second material and offset from a second side of the control electrode.

[0029] With the T-shape structure, adjacent devices can be fabricated while still maintaining a structure which results in termination of the strain relieving defects below the device area. Furthermore, an epi seam, as discussed herein above, is in the source/drain area which undergoes silicidation on the surface. Accordingly, no junction crosses the seam, so no leakage will be induced from any defects at the epi seam.

[0030] In another embodiment, the first current electrode can be formed in both the second material and a third portion of the first material, and the second current electrode can be formed in both the second material and a fourth portion of the first material. In a further embodiment, the control electrode is aligned vertically, overlying the at least one opening, thereby reducing floating body effects.

[0031] In yet another embodiment, the semiconductor device further includes a second dielectric layer overlying the dielectric layer. The second dielectric layer includes a different dielectric material than the first dielectric layer and is disposed adjacent the first current electrode and the second current electrode.

[0032] Still further, the semiconductor device can include a second opening in the dielectric layer, the second opening being filled with the first material and the overlying second material. In addition, the second opening includes an overlying second control electrode adjoined by a third current electrode and a fourth current electrode. The third current electrode is formed in direct physical contact with the second current electrode via a lateral extension of part of the second portion of the first material.

[0033] In still another embodiment, the semiconductor device further includes a second opening in the dielectric layer that is filled with the first material and the overlying second material. The second opening includes an overlying second control electrode adjoined by a third current electrode and a fourth current electrode. The first current electrode and the second current electrode are electrically isolated from the third current electrode and the fourth current electrode by the dielectric layer.

[0034] According to another embodiment, a semiconductor device comprises a single crystal substrate; an overlying dielectric layer having a first opening and a second opening with an overlying third opening that encompasses both the first opening and the second opening; a single crystal material filling the first opening, the second opening and a portion of the third opening, the single crystal material having controlled defects for relaxing strain at an

interface between the single crystal material and the substrate material existing only at interfaces in the first opening and the second opening, the single crystal material overlying controlled defect areas being substantially defect free; a single crystal strain material overlying the single crystal material and filling a remaining portion of the third opening, a thickness of the single crystal strain material being small enough to substantially avoid defect formation; a first transistor formed overlying and within at least the single crystal strain material and aligned to the first opening, the first transistor having a control electrode and first and second current electrodes; and a second transistor formed overlying and within at least the single crystal strain material and aligned to the second opening, the second transistor having a control electrode and first and second current electrodes, the first current electrode of the first transistor being in direct physical contact with the second current electrode of the second transistor allowing electrical interoperability between the first transistor and second transistor.

[0035] In the embodiment of the immediately preceding paragraph, the overlying dielectric layer further comprises: a first dielectric overlying the substrate that defines the first opening and the second opening; and a second dielectric that is a different material from the first dielectric that defines the third opening, the different material being used to avoid excessive etching of the first dielectric and second dielectric when making electrical contact to either the first current electrode or the second current electrode.

[0036] A method of forming an isolation structure in a semiconductor according to yet another embodiment of the present disclosure comprises: providing a single crystal substrate; forming a first dielectric overlying the substrate; forming a second dielectric overlying the first dielectric, the second dielectric being a different material than the first dielectric; forming a first opening having a first diameter completely through the first dielectric and forming a second opening having a second diameter completely through the second dielectric, the second diameter being equal to or greater than the first diameter wherein the first opening and the second opening expose a surface of the single crystal substrate; filling the first opening and a portion of the second opening with a first single crystal semiconductor material having a relaxed state by having defects for a controlled depth from the single crystal substrate to a predetermined height, a remainder of the first single crystal semiconductor material not having defects; filling a remaining portion of the second opening with a second single crystal semiconductor material that is strained by having a

predetermined thickness that does not exceed a critical thickness where defects begin to form; and forming a transistor overlying and within at least a portion of the second opening.

[0037] According to another embodiment, the method of the immediately preceding paragraph further comprises: forming the first opening to having a predetermined width and a predetermined depth, a ratio of the predetermined depth to the predetermined width being greater than one in order to define the controlled depth of defects of the first single crystal semiconductor material.

[0038] According to yet another embodiment, the method further comprises: using the different material of the second dielectric from the first dielectric as a control parameter to avoid excessive etching of the first dielectric and second dielectric when making electrical contact to a current electrode of the transistor.

[0039] Furthermore, the method further comprises: forming a third opening having a third diameter completely through the first dielectric and forming a fourth opening having a fourth diameter completely through the second dielectric, the fourth diameter being equal to or greater than the third diameter wherein the third opening and the fourth opening expose the surface of the single crystal substrate; and filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects; filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor and having a current electrode directly touching a current electrode of the first transistor.

[0040] The method of may also further comprise: forming a third opening having a third diameter completely through the first dielectric and forming a fourth opening having a fourth diameter completely through the second dielectric, the fourth diameter being equal to or greater than the third diameter wherein the third opening and the fourth opening expose the surface of the single crystal substrate; and filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by

having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects; filling a remaining portion of the fourth opening with a fourth single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor but not directly electrically connected to the first transistor.

[0041] According to yet another embodiment of the present disclosure, a method of forming an isolation structure in a semiconductor comprises: providing a single crystal substrate; forming a dielectric overlying the single crystal substrate; forming a first opening having a first diameter through a portion of the dielectric and forming a second opening having a second diameter through a remainder of the dielectric, the second diameter being equal to or greater than the first diameter wherein the first opening and the second opening expose a surface of the single crystal substrate; filling the first opening and a portion of the second opening with a first single crystal semiconductor material having a relaxed state by having defects for a controlled depth from the single crystal substrate to a predetermined height, a remainder of the first single crystal semiconductor material not having defects; filling a remaining portion of the second opening with a second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and forming a transistor overlying and within at least a portion of the second opening.

[0042] The method of the immediately preceding paragraph can further comprise: forming the first opening to having a predetermined width and a predetermined depth, a ratio of the predetermined depth to the predetermined width being greater than one in order to define the controlled depth of defects of the first single crystal semiconductor material.

[0043] The method may also further comprise: forming a third opening having a third diameter through a second portion of the dielectric and forming a fourth opening having a fourth diameter through a remainder of the second portion of the dielectric, the fourth diameter being equal to or greater than the third diameter wherein the third opening and the fourth opening expose the surface of the substrate; filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the

predetermined height, the remainder of the first single crystal semiconductor material not having defects; filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor and having a current electrode directly touching a current electrode of the first transistor.

[0044] Still further, the method may also comprise: forming a third opening having a third diameter through a second portion of the dielectric and forming a fourth opening having a fourth diameter through a remainder of the second portion of the dielectric, the fourth diameter being equal to or greater than the third diameter wherein the third opening and the fourth opening expose the surface of the substrate; filling the third opening and a portion of the fourth opening with the first single crystal semiconductor material having the relaxed state by having defects for a controlled depth from the single crystal substrate to the predetermined height, the remainder of the first single crystal semiconductor material not having defects; filling a remaining portion of the fourth opening with the second single crystal semiconductor material that is strained by having a predetermined thickness that does not exceed a critical thickness where defects begin to form; and forming a second transistor overlying and within at least a portion of the fourth opening, the second transistor being laterally adjacent the first transistor but not directly electrically connected to the first transistor.

[0045] Yet still further, according to one embodiment, the method further comprises: forming the first single crystal material with silicon germanium; forming the second single crystal material with silicon; forming the single crystal substrate with silicon; and forming the dielectric with one of silicon dioxide or silicon nitride.

[0046] In the foregoing specification, the disclosure has been described with reference to various embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present embodiments as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present embodiments.

[0047] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the term "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements by may include other elements not expressly listed or inherent to such process, method, article, or apparatus.